REMARKS

Applicants hereby request further consideration of the application in view of the amendments above and the comments that follow.

Status of the Claims

Claims 1-12 and 15 were pending in the application at the time of the Action. Claims 23 and 24 are newly added. Claims 1, 7-10 and 15 stand rejected under Section 102 (b) as being anticipated by U.S. Patent No. 6,090,708 to Sandhu et al. (Sandhu). Claim 10 has been rejected under statutory double patenting and objected to under 37 C.F.R. Section 1.75 as being a substantial duplicate of Claim 9.

Applicants appreciate the Examiner's indication that Claims 2-6 and 11-12 would be allowable if rewritten in independent form. Claim 11 has been rewritten in independent form. However, Applicants submit that independent Claims 1 and 15 are patentable over Sandhu for at least the reasons that follow. Applicants also traverse the Double Patenting rejection and objection of Claim 10 for the reasons that follow. Applicants submit that the current claims are in condition for allowance.

The Double Patenting Rejection and Objection under 37 C.F.R. § 1.75

Applicants respectfully submit that Claims 9 and 10 are not substantial duplicates as maintained on page 2 of the Action. Claim 9 recites "removing the capping layer on substantially the entire second side of the semiconductor substrate" and Claim 10 recites "removing the at least one layer on substantially the entire second side of the semiconductor substrate." Therefore, Claims 9 and 10 clearly relate to different elements of a substrate and recite different steps in the claimed methods. Claims 9 and 10 are not substantial duplicates of one another.

Accordingly, Applicants respectfully request that the rejection/objection to Claim 10 be withdrawn.

The Rejections under Section 102

Claim 1 is patentable over Sandhu

Independent Claim 1 recites a method of fabricating a semiconductor device. The method includes the following:

> forming at least one layer on a first and a second side of a semiconductor substrate;
> removing portions of the at least one layer on the first side of the semiconductor substrate to form a pattern of the at least one layer on the first side of the substrate while maintaining the at least one layer on the second side of the substrate;
> forming a capping layer on the pattern of the at least one layer on the first side of the substrate and on the at least one layer on the second side of the semiconductor substrate;
> removing the capping layer on the second side of the semiconductor substrate thereby exposing the at least one layer on the second side of the substrate while maintaining the capping layer on the first side of the substrate;
> removing the at least one layer on the second side of the semiconductor substrate, while maintaining the capping layer and the pattern of the at least one layer on the first side of the semiconductor substrate; and
> removing a portion of the capping layer on the first side of the semiconductor substrate.

Applicants respectfully submit that at least the underlined recitations are not taught or suggested by Sandhu.

On page 3 of the Action, the layer **20** of Sandhu (which Applicants assume includes the crystalline phase material layer **20*b*** shown in **Figure 11**) is identified as equivalent to the capping layer. As shown in **Figure 11** of Sandhu, the crystalline phase material layer **20*b*** is deposited on the semiconductive material layer **25** on one side of the substrate only. *See,* col. 7, lines 14-16 ("A crystalline phase material layer **20*b*** would be deposited into electrical connection with semiconductive material layer **25**..."). No mention is made of forming the layer **20*b*** on the other side of the substrate.

The Action further cites column 7, lines 20-28 as disclosing **both** "removing the at least one layer on the second side of the semiconductor substrate, while maintaining the

capping layer and the pattern of the at least one layer on the first side of the semiconductor substrate" and "removing the capping layer on the second side of the semiconductor substrate thereby exposing the at least one layer on the second side of the substrate while maintaining the capping layer on the first side of the substrate."

Column 7, lines 20-28 of Sandhu discusses forming a pattern of conductive line **30** on the top side of the substrate **12** and removing layer **18*b*** from the bottom side of the substrate.[1] If layer **18*b*** is considered by the Action to be equivalent to the at least one layer on the second side of the substrate as recited in Claim 1, then Sandhu does not teach or suggest removing the capping layer on the substrate second side. On the other hand, if layer **18*b*** is considered by the Action to be equivalent to the capping layer on the second side of the substrate as recited in Claim 1, then Sandhu does not disclose removing the at least one layer on the substrate second. Therefore, at least these recitations are not taught or suggested by Sandhu.

If the rejection is maintained, Applicants respectfully request that the specific portions and layers of Sandhu that are relied upon be clarified.

Accordingly, Applicants respectfully submit that Claim 1 is allowable over the cited art for at least the foregoing reasons. Claims 2-10 and new Claims 23 and 24 depend from Claim 1 and are therefore allowable as well for at least these reasons. The Examiner has also indicated that Claims 2-6 are allowable if rewritten in independent form. In addition, at least certain of the dependent claims are further distinguishable from the cited art as discussed below.

New Claims 23 and 24 are separately patentable

Claims 23 and 24 depend from Claim 1 and are patentable at least for the reasons discussed above. In addition, Claims 23 and 24 are separately patentable for at least the following reasons.

[1] Because Claim 1 recites "a pattern...on the first side of the substrate," for purposes of this discussion, it is assumed that the Action considers the top side of the substrate **12** of Sandhu to be equivalent to the substrate first side in Claim 1 and the bottom side of the substrate **12** to be equivalent to the substrate second side in Claim 1.

Claim 23 recites that "the pattern of the at least one layer on the first side of the substrate includes sidewalls, and the capping layer is formed on the sidewalls of the pattern." Support for Claim 23 can be found, for example, in Figures 6-8. In contrast, layer **20*b***, which the Action identifies as equivalent to the capping layer, is not formed on the sidewalls of the layer **25** as shown in **Figure 11** of Sandhu. Therefore, Claim 23 is separately patentable.

Claim 24 recites that "the capping layer is formed of a material that is different from the at least one layer on the second side of the substrate." Support for Claim 24 can be found, for example, on page 8, lines 2-4. Sandhu illustrates a single layer **18*b*** on the second side of the substrate **12**. Therefore, Claim 24 is separately patentable.

Claim 15 is patentable over Sandhu

Claim 15 recites a method for forming a memory device, the method including:

> forming a gate insulating layer on a first side and a second side of a semiconductor substrate;
>
> forming a gate electrode layer on the gate insulating layer on the first and the second sides of the semiconductor substrate;
>
> forming a masking layer on the gate electrode layer on the first and the second sides of the semiconductor substrate;
>
> patterning the gate insulating layer, the gate electrode layer and the masking layer on the first side of the semiconductor substrate to form a gate pattern on the first side of the semiconductor substrate while maintaining the gate insulating layer, the gate electrode layer, and the masking layer on the second side of the semiconductor substrate;
>
> forming a conductive layer on the gate pattern and on the first side of the substrate and on the masking layer on the second side of the semiconductor substrate;
>
> removing the conductive layer on the second side of the semiconductor substrate thereby exposing the masking layer;
>
> removing the masking layer, the gate electrode layer and the gate insulating layer on the second side of the semiconductor substrate while maintaining the conductive layer and the gate pattern on the first side of the semiconductor substrate; and
>
> removing a portion of the conductive layer on the first side of the semiconductor substrate to form contact pads between portions of the gate pattern.

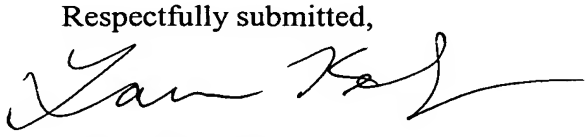
The Action states on page 4 that the layer **20** is equivalent to the conductive layer of Claim 15. However, as discussed above, the layer **20** is only formed on the top side of the substrate **12**. The Action cites column 7, lines 20-28 of Sandhu as disclosing **both** "removing the conductive layer on the second side of the semiconductor substrate" and "removing the masking layer, the gate electrode layer and the gate insulating layer on the second side of the substrate." Column 7, lines 20-28 of Sandhu discusses forming a pattern of conductive line **30** on one side of the substrate **12** and removing the layer ***18b*** on the other side of the substrate **12**. Assuming that the layer ***18b*** is considered by the Action to be equivalent to the conductive layer on the second side of the substrate (opposite the pattern), then Sandhu does not disclose removing the masking layer, the gate electrode layer and the gate insulating layer on the semiconductor second side as recited in Claim 15.

Accordingly, Sandhu cannot anticipate Claim 15 and Applicants respectfully submit that Claim 1 is allowable over the cited art for at least the foregoing reasons.

CONCLUSION

Applicants respectfully submit that this application is now in condition for allowance, which action is requested. Should the Examiner have any matters outstanding of resolution, he is encouraged to telephone the undersigned at 919-854-1400 for expeditious handling.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on December 9, 2005.

Carey Gregory